UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/047,754	01/14/2002	Varadarajan Srinivasan	002489.P036	5133

7590 02/07/2006

Daniel E. Ovanezian
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
VITAL, PIERRE M	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 02/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/047,754	SRINIVASAN, VARADARAJAN	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *37-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *37-51 and 53-58* is/are rejected.

7)☒ Claim(s) *52* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed December 22, 2005 in response to PTO Office Action mailed August 22, 2005. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, claims 37, 51, 53, 55 and 56 have been amended. Claims 1-36 have been previously canceled. No claims have been added. As a result, claims 37-58 remain pending in this application.

Response to Arguments

3. Applicant's arguments with respect to claims 37-58 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 37, 42-44, 46-48 and 53-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US Pub 2002/0126672) and Baum (US 5,619,713) in view of Khanna et al (US Pub 2003/0084236).

As per claim 37, Chow discloses a content addressable memory (CAM) apparatus comprising:

an array of CAM cells to store data to be compared with a comparand value (Fig. 1, element 106; Fig. 2, element 216; page 1, ¶ 9) ;

a select circuit to store a plurality of segment-select values, each segment-select value indicating which of a plurality of segments of input data is to source a respective bit of the comparand value (Fig. 2, elements 204 and 206; page 3, ¶ 37; page 4, ¶ 40); and

switch circuitry to output, as the comparand value, one or more bits of each of the plurality of segments of input data indicated by the select circuit to be a source of a bit of the comparand value (Fig. 2, element 204; page 4, ¶ 40-41).

Chow does not specifically teach that the select circuit stores a plurality of segment-select values, nor does Chow teach that the switch circuitry to output a bit in response to one of the select signals as required by claim 37.

Baum teaches a crosspoint switch (i.e. crossbar) for reordering the fields of a database record that is controlled by a plurality of select signals generated by a select

circuit (Fig. 17B, elements 1704, 1724 and 1725; column 30, lines 59-62; column 32, lines 16-18 and 42-48), where it readily apparent that the crosspoint switch outputs bytes in response to the select signals, and it is further noted that a byte comprises bits. Baum teaches that the field reordering is-useful for picking subsets of fields for easier pattern matching (column 30, lines 30-44).

Regarding claim 37, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the switch circuitry of Baum in the system of Chow, in order to pick subsets of fields for easier pattern matching.

Chow and Baum do not specifically teach a filter circuit to store data that indicates, within each of the plurality of segments indicated by the segment select values, selected bits, if any, to be included within the comparand value as required in the claim.

Khanna teaches an apparatus and method for generating a comparand in a CAM, wherein bit register position may be programmed with a value to either select or not select a corresponding bit group of input string for output to comparand register 460 (Page 4, ¶ 52; page 10, ¶ 112).

Further regarding claim 37, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the program register of Khanna as a

filter circuit in the system of Chow and Baum, in order to provide a comparand string that may be used to perform a lookup in the CAM (Page 4, ¶ 52) as taught by Khanna.

Claim 42 is rejected using the rationale derived from Chow and Baum and Khanna in the rejection of claim 37 above. However, Chow does not explicitly teach a program circuit coupled to the switch circuits for programming the switch circuits as required by claim 42.

Baum teaches a program circuit coupled to the switch circuits for programming the switch circuits in order to control the reordering of data through the switch (Fig. 17B, element 1724; column 32, lines 16-18 and 42-48).

Regarding claim 42, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to include a program circuit coupled to the switch circuits for programming the switch circuits as taught by Baum, in the system made obvious by the combination of Chow and Baum and Khanna as applied to claim 37 above, in order to control the reordering of data through the switch as taught by Baum.

Claim 43 is rejected according to the same rationale as for the rejection of claim 37 above.

Claim 44 is rejected using the rationale derived from Chow and Baum and Khanna in the rejection of claim 37 above. However, Chow does not explicitly teach a comparand register between the switch circuit and the array of CAM cells for storing a comparand value as required by claim 44.

Baum teaches a storage buffer for staging the data being reordered through the switch (Fig. 17B, element 1728; column 32, lines 52-65; column 34, lines 30-34), where it is noted that buffer is coupled between the switch and the next processing stage, and that buffering of data in this manner is well known in the art as a means for pipelining operations in a system.

Regarding claim 44, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to store the data being reordered through the switch in a buffer coupled between the switch and the next processing stage (i.e. the array of CAM cells) as taught by Baum, in the system made obvious by the combination of Chow and Baum as applied to claim 37 above, in order to allow a pipelined operation of the system.

As in claim 46, Chow teaches that the position of a bit may change between the input data and the comparand value (Figs. 7A and 7B; page 5, ¶ 49-51).

Claim 47 is rejected according to the same rationale as for the rejection of claim 37 above, noting that a CAM stores data in a matrix of cells (inherently, a CAM comprises a plurality of rows).

Claim 48 is rejected according to the same rationale as for the rejection of claim 37 above.

Claim 53 is rejected according to the same rationale as for the rejection of claim 37 above.

Claim 54 is rejected according to the same rationale as for the rejection of claim 43 above.

Claim 55 is rejected according to the same rationale as for the rejection of claim 37 above. Chow discloses that the comparand is compared with data in the CAM (Page 4, ¶ 40), where the lookup operation in the CAM is understood to compare the input key (i.e. comparand) with data stored in the CAM.

As to claim 56, the rationale derived from Chow and Baum and Khanna in the rejection of claim 37 is applied herein. However, the combination of Chow and Baum and Khanna as applied to claim 37 does not teach receiving a plurality of segments of

input data and enabling the programmed switch circuitry in response to the segment information as required by claim 56.

Baum further teaches that a complete record of input data may be operated on sequentially by dividing the record into a number of quadwords (i.e. segments), and that the switch is enabled in response to segment information (i.e. i-counter value) indicating which segment of the input data is received at any given time (Figs. 17B, 18A-18C; column 34, lines 11-56). One skilled in the art would recognize that the sequential approach of Baum allows extraction and assembly operations to be performed on an input data record wider than the processing circuitry width, thereby trading off speed of computation for conservation of circuit area.

Regarding claim 56, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to receive a plurality of input data segments and to selectively enable the switch in response to segment information indicative of the particular segment of input data as taught by Baum, in the system of Chow and Baum and Khanna as applied to claim 37 above, in order to trade off speed of computation for conservation of circuit area.

Claim 57 is rejected according to the same rationale as for the rejection of claim 56 above.

As in claim 58, Chow discloses that the comparand is compared with data in the CAM (Page 4, ¶ 40), where the lookup operation in the CAM is understood to compare the input key (i.e. comparand) with data stored in the CAM.

6. Claims 38-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US Pub 2002/0126672) in view of Baum (US 5,619,713) and Khanna et al (US Pub 2003/0084236) and further in view of Ninomiya (US 5,809,330).

Chow and Baum and Khanna are relied upon for the teachings relative to claim 37 as above, where it is further noted that in the select circuit of Baum a counter provides input segment information to a decoder for generating the select signals to the crossbar switch (Fig. 17B, elements 1725 and 1731; column 32, lines 59-65).

The combination of Chow and Baum and Khanna does not teach that the select circuit comprises a memory element for storing programmed segment information, and a compare circuit to compare the programmed segment information with the input segment information to generate a select signal as required by claim 38.

Ninomiya teaches a programmable decoder for generating select signals comprising memory elements for storing programmed information, and compare circuits

to compare the programmed information with input information to generate a select signal (Fig. 4; column 9, line 59 to column 10, line 5). Ninomiya suggests that making the decoder programmable enables the flexibility of changing the decoder behavior with a simple update to the stored program information (column 3, lines 42-49).

Regarding claim 38, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the decoder of Ninomiya, to generate the select signals for the crossbar switch in the system made obvious by the combination of Chow and Baum and Khanna, in order to provide the flexibility of being able to change the decoding behavior as taught by Ninomiya.

Regarding claim 39, the combination of Chow and Baum and Khanna also does not teach that the memory element and compare circuit form a CAM cell as required by claim 3.

Regarding claim 39, Ninomiya teaches memory elements paired with compare circuits (Fig. 4; column 9, line 59 to column 10, line 5).

One of ordinary skill in the art would readily recognize that a memory element paired with a compare circuit comprises a CAM cell and therefore it would have been obvious to group these elements together in order to realize an area efficient design.

7. Claims 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US Pub 2002/0126672) in view of Baum (US 5,619,713) and Khanna et al (US Pub 2003/0084236) and further in view of Reblewski (US Pub 2003/0 131331).

Chow and Baum and Khanna are relied upon for the teachings relative to claim 37 as above, where it is further noted that Chow teaches selecting bits individually from the input data (Figs. 7A-7B; page 5, ¶ 49-51) while Baum teaches selecting bits as groups of bytes (Column 32, lines 42-49).

The combination of Chow and Baum and Khanna does not teach an L-bit by L-bit switch with L select signals as required by claim 40.

Reblewski teaches a generic crossbar device where there is a one to one correspondence between the select signals, input data bits, output data bits (i.e. L-bit by L-bit switch with L select signals) (Figs. 1a -1b; page 1, ¶ 5, lines 1-7), where it is noted that the select signals are provided by memory elements corresponding to the switches.

It is readily apparent that using a one to one correspondence between the select signals, input data bits and the output data bits enables fine-grained switching that allows manipulation of input data fields as small as one bit as taught by Chow.

Regarding claim 40, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use a one to one correspondence between select signals, input data bits and output data bits as taught by Reblewski, in the system made obvious by the combination of Chow and Baum and Khanna, in order to enable the fine-grained switching that allows manipulation of single bit data fields as taught by Chow.

The combination of Chow, Baum and Khanna and Reblewski as applied to claim 40 above, does not teach that the L input data bits are one of N segments of M input bits, where M is equal to N multiplied by L as required by claim 41. However, Baum further teaches that a complete record of input data (i.e. M input bits) may be operated on sequentially by dividing the record into a number (i.e. N segments) of quadwords (i.e. L input data bits) (Figs. 17B, 18A-18C; column 34, lines 11-56). One skilled in the art would recognize that the sequential approach of Baum allows extraction and assembly operations to be performed on an input data record wider than the processing circuitry width, thereby trading off speed of computation for conservation of circuit area.

Regarding claim 41, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to divide M input bits into N segments of L input data bits as taught by Baum, in the system of Chow, Baum, Khanna and Reblewski as applied to claim 40 above, in order to trade off speed of computation for conservation of circuit area.

8. Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US Pub 2002/0126672) in view of Baum (US 5,619,713) and Khanna et al (US Pub 2003/0084236) as applied to claim 44 above, and further in view of Gandini (US 6,169,685).

Chow, Baum and Khanna are relied upon for the teachings relative to claim 44 as above.

The combination of Chow and Baum and Khanna does not teach a global mask register coupled to the comparand storage element and the array of CAM cells as required by claim 45.

Gandini teaches a CAM memory where a global mask register is coupled to a comparand register and an array of CAM cells in order to indicate comparand indifference conditions (Fig. 1, elements "RE" and "MA"; column 3 lines 36-46).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the global mask register as taught by Gandini, in the system of Chow and Baum and Khanna, in order to indicate comparand indifference conditions as taught by Gandini.

9. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US Pub 2002/0126672) in view of Baum (US 5,619,713) and Khanna et al (US Pub 2003/0084236) as applied to claim 47 above, and further in view of Patti et al (US 2001/0048625).

The rationale derived from the combination of Chow and Baum and Khanna in the rejection of claim 47 above is incorporated herein. The combination of Chow and Baum and Khanna does not teach that the rows are segmented to form a plurality of columns of row segments as required by claim 50.

Patti teaches a reconfigurable memory including an array of memory storage cells wherein the blocks may be viewed as a partitioning of the rows into a sequence of blocks thereby allowing each block to have bit lines that operates independently of the bit lines of other blocks (page 3, ¶ 32).

Regarding claim 50, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use rows segmented to form a plurality of columns of row segments as taught by Patti in order to allow each block to have bit lines that operates independently of the bit lines of other blocks (page 3, ¶ 32) as taught by Patti.

10. Claims 49 and 51 rejected under 35 U.S.C. 103(a) as being unpatentable over Chow (US Pub 2002/0126672) in view of Baum (US 5,619,713) and Khanna et al (US Pub 2003/0084236) as applied to claim 47 above, and further in view of Kansal et al (US 6,374,326).

The rationale derived from the combination of Chow and Baum and Khanna in the rejection of claim 47 above is incorporated herein. The combination of Chow and Baum and Khanna does not teach an integer plurality of the above system as required by claim 49.

Kansal teaches an integer plurality of CAM arrays for performing concurrent lookup operations (Figs. 2 and 3; column 1, line 66 to column 2, line 13). It is noted that although Kansal shows the comparand generation as a single functional unit (Figs. 2 and 3A, element 260), Kansal teaches the generation of a unique comparand for each lookup (Column 2, lines 14- 23).

Regarding claim 49, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use a plurality of CAM lookup systems as taught by Kansal, where the CAM systems are embodied by the combination of Chow and Baum and Khanna, in order to perform concurrent lookup operations as taught by Kansal.

Claim 51 is rejected according to the same rationale as for the rejection of claim 49 above.

Allowable Subject Matter

11. Claim 52 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record does not teach or suggest "the number of CAM cells included in each row segment matches a width of the comparand value and wherein the switch circuitry is coupled to provide the comparand value to each of the plurality of columns of row segments" in combination with the other element set forth in the claimed invention.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider these references fully when responding to this action. The documents cited therein teach input data selection for content addressable memory.

15. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

16. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the

art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (571) 272-4215. The examiner can normally be reached on 8:30 am - 6:00 pm, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

February 2, 2006

PIERRE VITAL
PRIMARY EXAMINER